#4

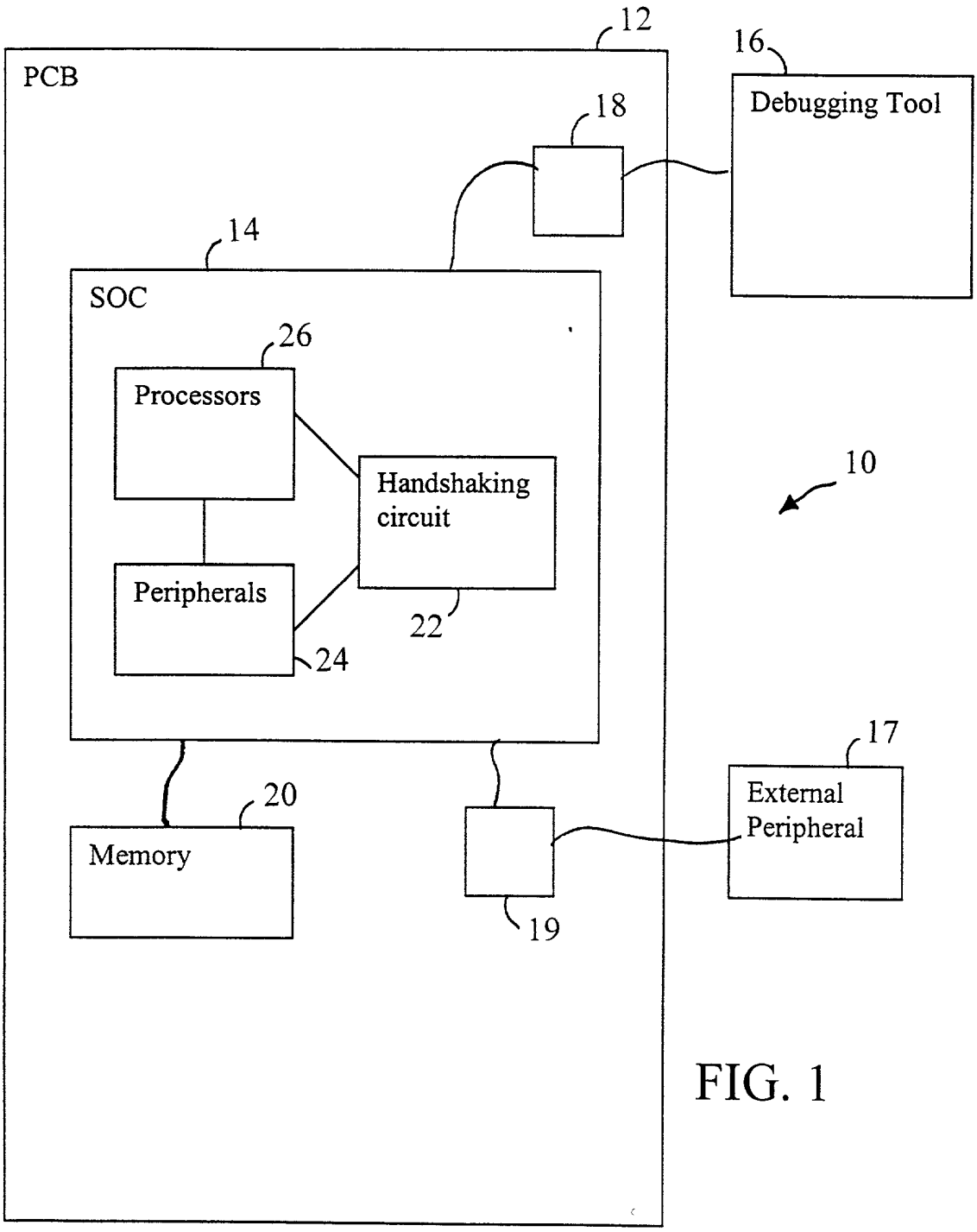
12
PCB
16
Debugging Tool
18
14
SOC
26
Processors
Handshaking circuit
10
Peripherals
22
24
17
External Peripheral
20
Memory
19

FIG. 1

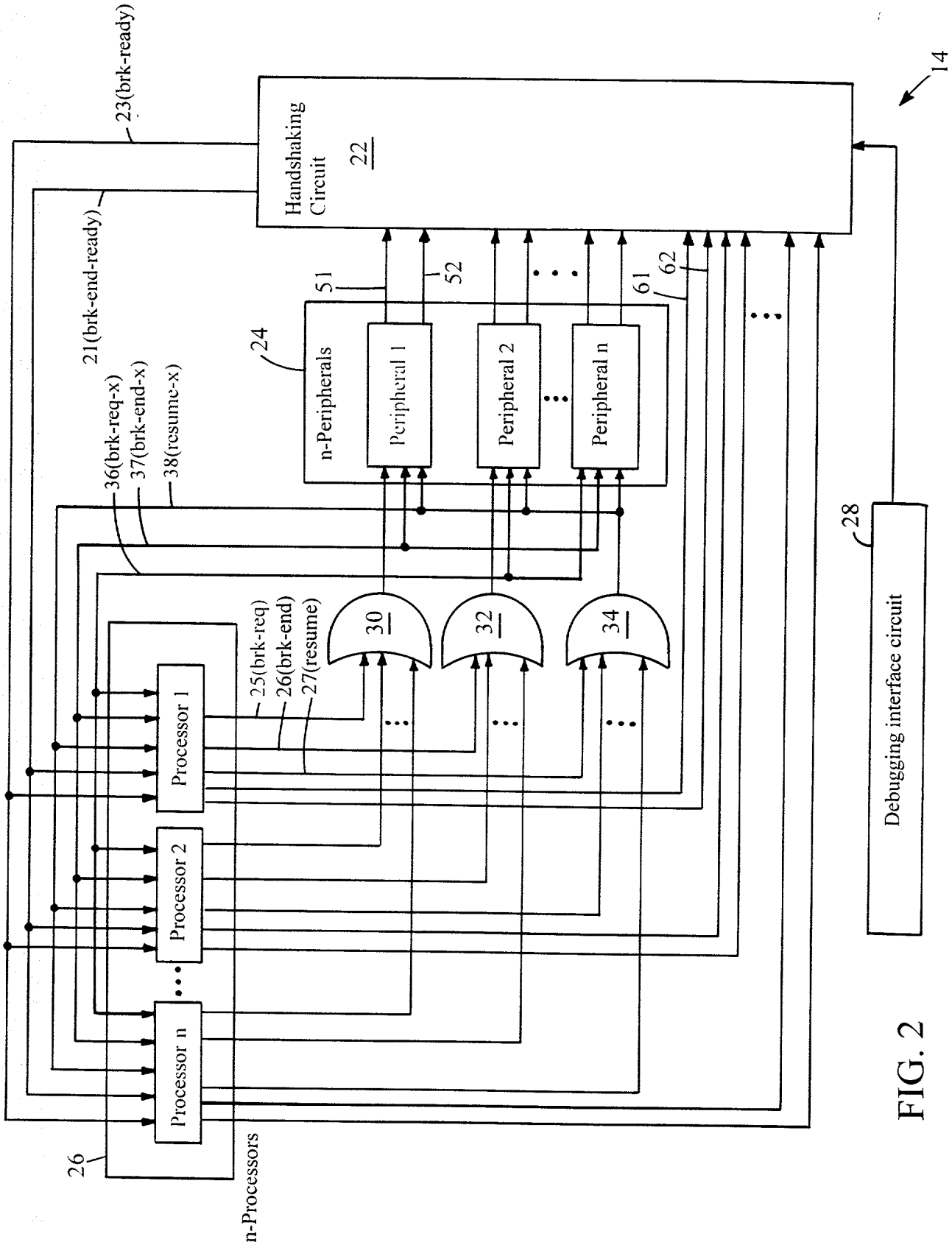
14
Handshaking Circuit
22
23(brk-ready)
21(brk-end-ready)
36(brk-req-x)
37(brk-end-x)
38(resume-x)
24
n-Peripherals
Peripheral 1
Peripheral 2
Peripheral n
51
52
61
62
28
Debugging interface circuit
30
32
34
25(brk-req)
26(brk-end)
27(resume)
Processor 1
Processor 2
Processor n
26
n-Processors

FIG. 2

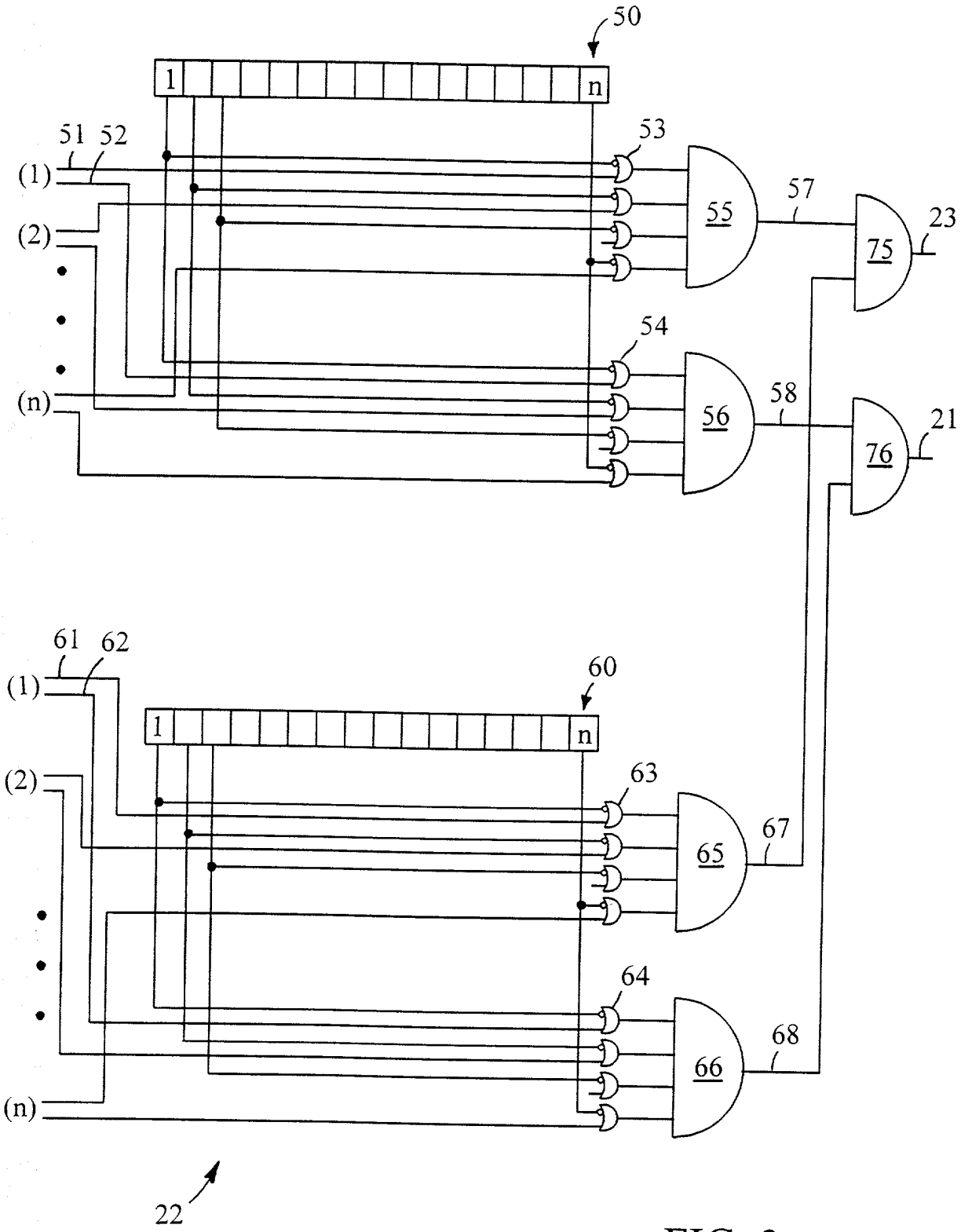
50
1
n
51
52
53
(1)
(2)
(n)
55
57
75
23
54
56
58
76
21
61
62
60
1
n
63
65
67
64
66
68
(1)
(2)
(n)
22

FIG. 3

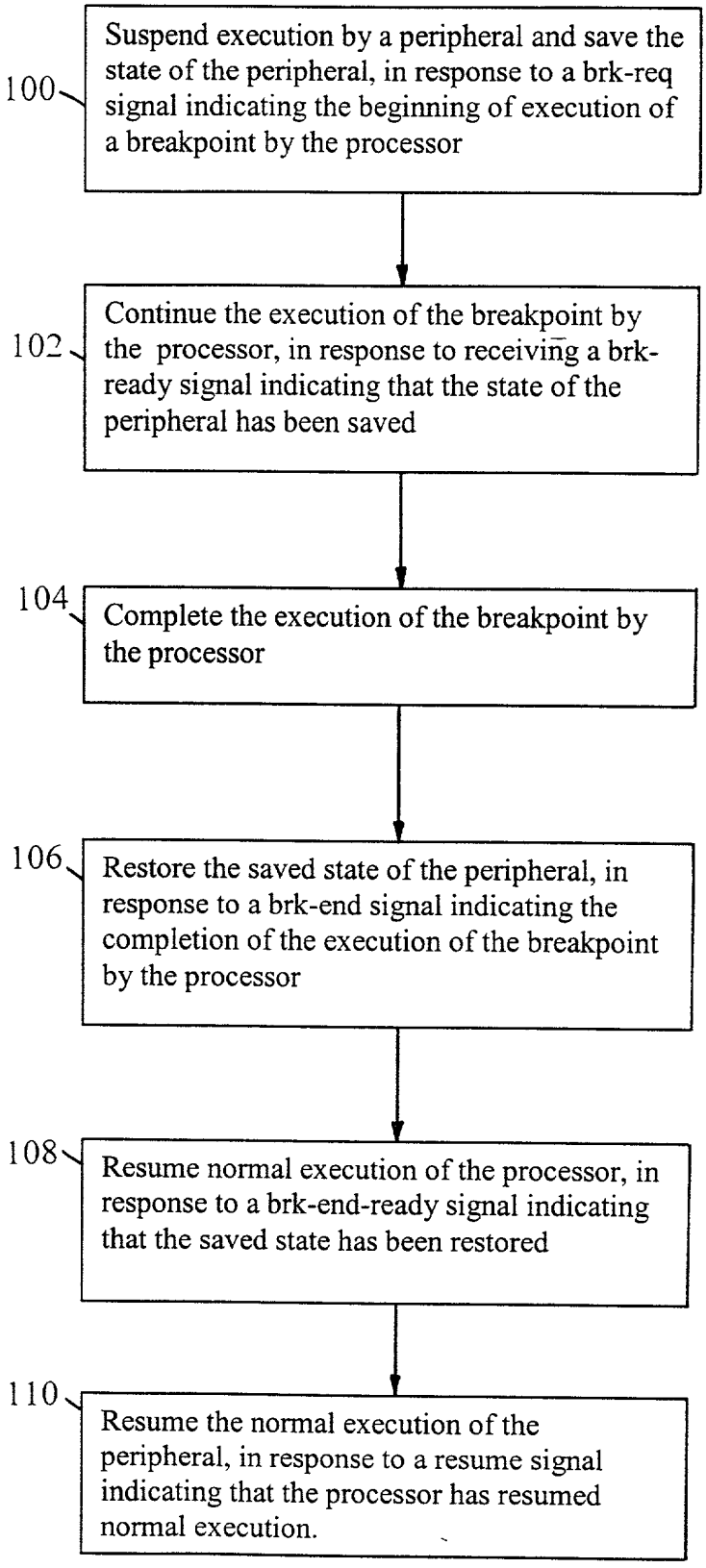
100
Suspend execution by a peripheral and save the state of the peripheral, in response to a brk-req signal indicating the beginning of execution of a breakpoint by the processor
102
Continue the execution of the breakpoint by the processor, in response to receiving a brk-ready signal indicating that the state of the peripheral has been saved
104
Complete the execution of the breakpoint by the processor
106
Restore the saved state of the peripheral, in response to a brk-end signal indicating the completion of the execution of the breakpoint by the processor
108
Resume normal execution of the processor, in response to a brk-end-ready signal indicating that the saved state has been restored
110
Resume the normal execution of the peripheral, in response to a resume signal indicating that the processor has resumed normal execution.

FIG. 4